AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A computer system comprising:

a chipset including a bus-IO controller, a memory controller and a first video controller;

a second video controller coupled to the chipset;

~~at least one~~ a display device coupled to the video controllers;

a switching device included in the chipset configured to receive ~~analog and digital~~ video signals from either of the video controllers at respective inputs and to provide the signals to a compatible display device; and

the switching device being coupled to a ~~respective~~ connector for ~~each~~ the display device;

~~wherein the chipset includes an AGP port, and wherein the second video controller is configured to provide a compatible signal to the switching device using the AGP port.~~whereby the second video controller provides its video signals to the switching device through the chipset via an AGP port.

2. (Cancelled).

3. (Cancelled).

4. (Cancelled)

5. (Cancelled).

6. (Currently Amended) The computer system of claim 1, further comprising:

a processor coupled to the chipset; and

a system memory configured to store a program that is executable by the processor;

wherein the program includes instructions for causing the switching device to provide the first signal or the second signal to the ~~first~~ display device.

7. (Cancelled).

8. (Cancelled).

9. (Previously Presented) The computer system of claim 1, wherein the signals include analog and digital signals.

10. (Currently Amended) A computer system comprising:

a chipset including a bus-I/O controller, a memory controller and a first video controller;

an interface coupled to the chipset and configured to receive a second video controller;

~~at least one~~ a display device coupled to the video controllers;

a switching device included in the chipset coupled to receive ~~analog and digital~~ video signals from either of the video controllers at respective inputs and to provide the signals to a compatible device; and

the switching device being coupled to a ~~respective~~ connector for ~~each~~ the display device;

~~wherein the chipset includes an AGP port, and wherein the AGP port is configured to receive a compatible signal from the second video controller.~~whereby the second video controller provides its video signals to the switching device through the chipset via an AGP port.

11. (Cancelled).

12. (Cancelled).

13. (Cancelled).

14. (Cancelled).

15. (Currently Amended) The computer system of claim 10, further comprising:

a processor coupled to the chipset; and

a system memory configured to store a program that is executable by the processor;

wherein the program includes instructions for causing the switching device to provide ~~the first~~ a signal from the first video controller to the ~~first~~ display device in response to the second video controller not being coupled to the interface, and wherein the program includes instructions for causing the switching device to provide ~~the second~~ a signal from the second video controller to the ~~first~~ display device in response to the second video controller being coupled to the interface.

16. (Cancelled).

17. (Cancelled).

18. (Previously Presented) The computer system of claim 10, wherein the signals include analog and digital signals.

19. (Cancelled).

20. (Cancelled).

21. (Currently Amended) A method of providing a video signal to a display device in a scalable platform comprising:

providing a chipset including a bus-I/O controller, a memory controller and a first video controller;

providing a second video controller coupled to the chipset;

providing ~~at least one~~ a display device coupled to the video controllers;

configuring a switching device included in the chipset to receive ~~analog and digital~~ video signals at respective inputs from either of the video controllers and to provide each of the signals to a compatible display device; and

~~wherein the chipset includes an AGP port and wherein the second video controller is configured to provide a compatible signal to the switching device using the AGP port.~~ the second video controller providing its video signals to the switching device through the chipset via an AGP port.